Abstract of the Disclosure:

The circuit has a first input for supplying a first signal (S1) to a series circuit made from a plurality of basic elements. Each basic element has a memory (M) for storing the signal level which is applied to the input of the basic element, and the output of a storage element (M) is connected to the input of a next basic element. Furthermore, the circuit has a second input for supplying a second signal (S2) which is connected to a control input of each basic element. Given a first level of the second signal, the storage elements (M) take up the signal level stored in the preceding storage element, and given a second level of the second signal, the storage elements (M) retain the signal level respectively stored in them. Furthermore, the circuit has comparator units (XOR) to which, in each case, the signal levels stored by the storage units (M) of two adjacent basic elements are supplied.

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